REMARKS

Claims 1-8, 13, 14 and 20-33 re pending in this application. By this Amendment, claims 1, 6, 23-26 are amended, and claims 32 and 33 are added. No new matter is added.

The courtesies extended to Applicant's representative by Examiners Sherman and Awad at the interview held May 7, 2007, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicants' record of the interview.

I. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1-3, 6-8, 13, 14, 20, 22-24 and 28-31 under 35 U.S.C. §102(e) over U.S. Patent Application Publication No. 2003/0052614 to Howard; rejects claims 4 and 5 under 35 U.S.C. §103(a) over Howard in view of U.S. Patent No. 6,229,506 to Dawson; and rejects claims 21, 25 and 26 under 35 U.S.C. §103(a) over Howard in view of U.S. Patent Application Publication No. 2003/0058195 to Adachi et al. These rejections are respectfully traversed.

As agreed during the personal interview, none of the applied references teaches or suggests "no current flowing through the first transistor during the second period," as recited in independent claim 1 (emphasis added). Similarly, none of the applied references teaches or suggests "no current flowing through a transistor included in one unit circuit of the plurality of unit circuits during a second period in which the voltage signal is supplied to the one unit circuit," as recited in independent claim 6 (emphasis added). Further, none of the applied references teaches or suggests "no current flowing through the first transistor during the second period," as recited in independent claims 23, and as similarly recited in independent claim 24 (emphasis added).

As agreed during the personal interview, Howard discloses a current flowing through the transistor during a second period, for example, at paragraph [0029].

Further, Dawson and Adachi do not remedy the deficiencies of Howard. Dawson is only cited by the Office Action for its alleged teaching of a transistor that controls a timing to start or stop a supply of current, and a transistor wherein the amount of charge held in a capacitor is reset to a predetermined state when the transistor is turned on. Further, Adachi is only cited by the Office Action for its alleged teaching of a data current being a multi-value data current.

Thus, for at least these reasons, independent claims 1, 6, 23 and 24 are patentable over the applied references. Further, claims 2-5, 7, 8, 13, 14, 20-22 and 25-31, which variously depend from claims 1, 6, 23 and 24, are also patentable over the applied references for at least the reasons discussed above, as well as for the additional features they recite. Withdrawal of the rejections is thus respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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JAO:RBI/hms

Date: May 21, 2007

Attachment:
Amendment Transmittal

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